SESSION 17 – Honolulu Suite
Process Technology

Thursday, June 17, 8:00 a.m.
Chairpersons: S. Broydo, SB Associates
Y. Tada, Tokyo Electron AT

17.1 — 8:00 a.m.
Novel Fabrication Process to Realize Ultra-thin (EOT = 0.7nm) and Ultra-low Leakage SiON Gate Dielectrics, D. Matsushita, K. Muraoka, Y. Nakasaki, K. Kato, S. Inumiya, K. Eguchi and M. Takayanagi, Toshiba Corporation, Yokohama, Japan

We achieved 0.73 nm EOT, 88 A/cm2 Jg, and 92% Gm of that for SiO2 by just oxidation of SiN films. In addition, we achieved further improvement of EOT-Jg characteristics by re-nitridation process with minimum degradation of Gm. EOTof 0.70 nm and Jg as 95 A/cm2 is realized with superior suppression of boron penetration (delta Vth=0.04 V).

17.2 — 8:25 a.m.
Ultra-Shallow Junction Formation by Non-Melt Laser Spike Annealing for 50-nm Gate CMOS, A. Shima, Y. Wang*, S. Talwar* and A. Hiraiwa, Hitachi, Ltd., Tokyo, Japan, *Ultratech, Inc., San Jose, CA

We activated source/drain junctions of CMOS by simply replacing RTA in the conventional production flow by non-melt laser spike annealing (LSA). We formed no additional layers unlike the conventional laser annealing. The 50-nm gate CMOS devices thus formed had better Vth roll-offs and larger drain currents compared to those by RTA. We found that the optimization of the overlap length between the gate and source/drain extensions was important due to the minimal lateral diffusion during the sub-millisecond annealing of LSA.

17.3 — 8:50 a.m.
Extended Scaling of Ultrathin-Gate Oxynitride Toward Sub-65nm CMOS by Optimization of UV Photo-Oxidation, Soft Plasma/Thermal Nitridation & Stress Enhancement, C.-C. Chen, V.S. Chang, Y. Jin, C.-H. Chen, T.-L. Lee, S.-C. Chen and M.-S. Liang, Taiwan Semiconductor Manufacturing Co., Ltd., Hsin-Chu, Taiwan, ROC

A novel UV photo-oxidation is developed for ideal “atomic-layer oxidation” with excellent thickness control down to 4Å, which is very promising for interfacial layer formation of scaled oxynitride and high-*k* applications. Ultra thin oxynitride using newly-developed low ion-energy nitrogen plasma (30% damage reduction) combining with thermal nitridation is demonstrated for n/pFET optimization. Device performance is further enhanced by stress modulation from strain contact-etch-stop layer. The proposed technologies represent an efficient approach to realize ultra thin oxynitride toward sub-65nm CMOS production.

17.4 — 9:15 a.m.
Ultra-Low Cost and High Performance 65nm CMOS Device Fabricated with Plasma Doping, F. Lallement, B. Duriez*, A. Grouillet, F. Arnaud, B. Tavel*, F. Wacquant, P. Stolk*, M. Woo**, Y. Erokhin***, J. Scheuer***, L. Godet***, J. Weeman***, D. Distaso*** and D. Lenoble, STMicroelectronics, Crolles, France, *Philips Semiconductors, **Motorola, Inc., ***Varian SEA

Plasma Doping (PLAD) process have been developed for fabricating the ultra-shallow junctions (USJ) needed for the 65nm CMOS technology. The benefit of PLAD versus ultra-low energy implantations is demonstrated with a standard spike annealing activation. Such plasma-doped USJ were successfully integrated into a conventional 65nm CMOS architecture (no offset spacers). Transistors drive currents of 720 and 330 µA/µm for NMOS and PMOS respectively are obtained (Vdd=0.9V, Ioff=100 nA/µm). Junction leakage and capacitance were also improved.

17.5 — 9:40 a.m.
B_2H_6 Plasma Doping with "*In-situ* He Pre-amorphization", Y. Sasaki, C. G. Jin, H. Tamura, B. Mizuno, R. Higaki*, T. Satoh*, K. Majima*, H. Sauddin*, K. Takagi*, S. Ohmi*, K. Tsutsui*, and H. Iwai*, Ultimate Junction Technologies, Osaka, Japan, *Tokyo Institute of Technology, Tokyo, Japan

Plasma doping process to reduce Rs keeping shallow Xj was demonstrated. In-situHelium pre-amorphization (He-PA) was introduced to plasma doping method. High dose and ultra-shallow as doped profiles were optimized by adjusting B2H6 PD conditions. The optical absorbtion rate in the amorphous layer and Xj was controlled by the He-PA conditions. Advantage of these new techniques to form ultra-shallow p+-n junction were verified by Flash lamp annealing and Laser annealing for the first time.